M SQUARE MIPI PHY IP

WHITE PAPER

Overview

M SQUARE MIPI C/D-PHY IP enables high performance, low power interface between system on chips (SOC) and peripheral devices. The target market covers wide range of IoT application areas including automotive ADAS and infotainment, VR/AR, multimedia, digital cameras and image sensors etc. Our IP includes both transmitter and receiver and is available in both mainstream and advanced process nodes such as 16/12nm, 28/22nm and 65-40nm. This high quality, low cost and interoperable IP enables end customers to deploy specific features for their applications.

This IP is designed to transmit data and the control information of MIPI CSI, DSI, or other associated protocols. For MIPI C-PHY operation, this IP comprises up to three trios for single-channel configuration and interfaces with MIPI-associated protocol controllers via a standard MIPI C-PHY PPI which supports 16-bit or 32-bit high speed transmitting data bus. This IP can also be configured as MIPI D-PHY transmitter/receiver interface. For MIPI D-PHY operation, this IP comprises one clock lane and up to four data lanes for single-channel configuration.

Highlights

Complies with MIPI D-PHY v1.2 and C-PHY v1.2 Specs
Supports MIPI DSI and CSI-2 protocols
Supports high speed data rate up to 2.5Gbps per lane for D-PHY and 3.5Gsps per trio for C-PHY
Supports low speed data rate of 10Mbps and ultra-low-power mode
Supports D-PHY mode with 1 clock lane and up to 4 data lanes
Supports C-PHY mode up to 3 trios for TX and 4 trios for RX
Supports TX-EQ function to compensate loss of long channel
Provides D-PHY swap function for clock and data lanes
Provides C-PHY swap function for trios
Provides a stand-alone at-speed multi-lanes (trios) parallel BIST module for mass production test

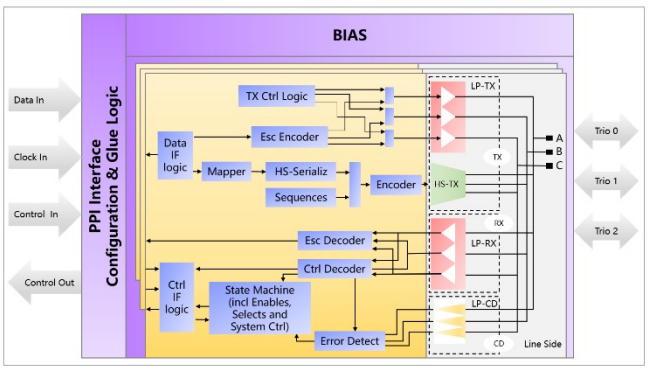

Figure 1: Block Diagram of MIPI C/D PHY Combo TX

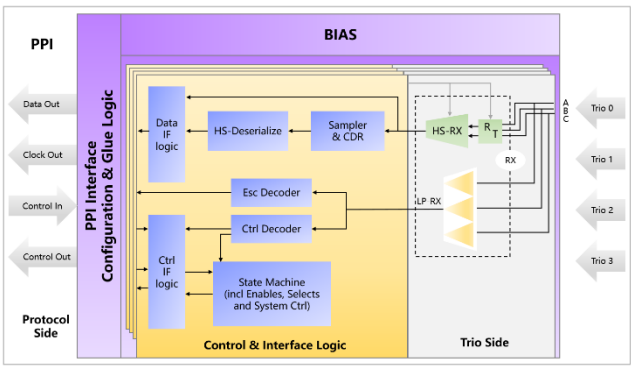

Figure 2: Block Diagram of MIPI C/D PHY Combo RX

www.m2ipm2.com marcom@m2ipm2.com 6F, Building No. 6-2, No. 519 Shenchang Rd, Minhang, Shanghai, 201107.